AMENDMENTS TO THE CLAIMS

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1-2. (Canceled)

3. (Previously Presented) A microcomputer comprising:

an oscillation circuit which oscillates and outputs an oscillation signal and stops the oscillation during a period in which it receives an oscillation stop signal;

a wakeup terminal that receives from outside a wakeup signal of a predetermined cycle; and

a clock control circuit which receives the wakeup signal, outputs the oscillation stop signal, and stops output of the oscillation stop signal based on the wakeup signal, and which receives the oscillation signal from said oscillation circuit and generates a main clock based on the oscillation signal.

4. (Canceled)

5. (Original) The microcomputer according to claim 3, wherein said clock control circuit nullifies the wakeup signal received when the oscillation signal is output from said oscillation circuit.

6. (Original) The microcomputer according to claim 3, further comprising a register which stores history information related to the executed commands as register value,

wherein when said clock control circuit stops output of the oscillation stop signal, processing is executed from an instruction immediately following the instruction that was executed just before stopping the oscillation of said oscillation circuit based on a value stored in said register just before stopping the oscillation of said oscillation circuit.

7. (Original) The microcomputer according to claim 3, further comprising an interrupt control circuit to which the signal is input as an interrupt requesting signal for executing an interrupt processing,

wherein when the oscillation of said oscillation circuit is stopped when a permission for a request for an external interrupt has been given, and further if said clock control circuit stops output of the oscillation stop signal, said interrupt control circuit executes the signal representing the permission for the request for the interrupt is input into said interrupt control circuit.

8. (Original) The microcomputer according to claim 7, wherein the microcomputer is a one-chip microcomputer equipped with said oscillation circuit, clock control circuit, and said interrupt control circuit on the same LSI chip.

9. (Original) The microcomputer according to claim 3, further comprising an address generating circuit which receives the wakeup signal and outputs, based on the

wakeup signal, a specific address corresponding to which a specific processing is to be performed,

wherein said address generating circuit outputs the specific address when said clock control circuit stops output of the oscillation stop signal.

10. (Original) The microcomputer according to claim 9, wherein the microcomputer is a one-chip microcomputer equipped with said oscillation circuit, clock control circuit, and said interrupt control circuit on the same LSI chip.

11. (Original) The microcomputer according to claim 3, wherein said clock control circuit receives the oscillation signal and outputs the oscillation stop signal based on a condition of the oscillation signal.

12. (Previously Presented) A microcomputer comprising:

an oscillation circuit which oscillates and outputs an oscillation signal and stops the oscillation during a period in which it receives an oscillation stop signal;

a wakeup terminal that receives from outside a wakeup signal of a predetermined cycle; and,

a clock control circuit which receives the wakeup signal, outputs the oscillation stop signal to said oscillation circuit only for a specific time interval based on the wakeup signal, and receives the oscillation signal from said oscillation circuit and generates a main clock based on the oscillation signal.

13. (Original) The microcomputer according to claim 12, wherein said clock control circuit receives the oscillation signal and outputs the oscillation stop signal based on a condition of the oscillation signal.

14. (Previously Presented) A microcomputer comprising:

an oscillation circuit which oscillates and outputs an oscillation signal and stops the oscillation during a period in which it receives an oscillation stop signal;

a wakeup terminal that receives from outside a wakeup signal of a predetermined cycle; and

a clock control circuit which receives the wakeup signal and the oscillation signal, outputs the oscillation stop signal to said oscillation circuit only for a specific time interval based on the wakeup signal and the oscillation signal, and generates a main clock based on the oscillation signal.

15. (Original) The microcomputer according to claim 14, wherein said clock control circuit outputs the oscillation stop signal based on a condition of the oscillation signal.

16. (Previously Presented) A microcomputer comprising:

an oscillation circuit which oscillates and outputs an oscillation signal;

a wakeup terminal that receives from outside a wakeup signal of a predetermined cycle; and

a clock control circuit which receives the wakeup signal and the oscillation signal,

wherein said clock control circuit monitors a condition of the oscillation signal and outputs the oscillation stop signal to said oscillation circuit based on the condition of the oscillation signal thereby stopping the oscillations of said oscillation circuit, and wherein said clock control circuit generates a main clock based on the oscillation signal, and,

when said oscillation circuit is not oscillating and when specific time has lapsed, said clock control circuit stops output of the oscillation stop signal to said oscillation circuit based on the wakeup signal.

17. (Original) The microcomputer according to claim 16, wherein said clock control circuit outputs the oscillation stop signal when it does not receive the oscillation signal.

18. (Previously Presented) A microcomputer system comprising:

a wakeup signal supplying unit that generates a wakeup signal of a predetermined cycle; and

a microcomputer, said microcomputer including,

an oscillation circuit which oscillates and outputs an oscillation signal;

a wakeup terminal that always receives the wakeup signal of a predetermined cycle from said wakeup signal supplying unit; and

a clock control circuit which controls said oscillation circuit so as to stop the oscillation, and based on the wakeup signal received through said wakeup terminal controls said oscillation circuit so as to restart the oscillation, and receives the oscillation

signal from said oscillation circuit and generates a main clock based on the oscillation signal.

19. (Previously Presented) A microcomputer system comprising:

a wakeup signal supplying unit that generates a wakeup signal of a predetermined cycle; and

a microcomputer, said microcomputer including,

an oscillation circuit which oscillates and outputs an oscillation signal and stops the oscillation during a period in which it receives an oscillation stop signal;

a wakeup terminal that always receives the wakeup signal of a predetermined cycle from said wakeup signal supplying unit; and

a clock control circuit which receives the wakeup signal, outputs the oscillation stop signal, and stops output of the oscillation stop signal based on the wakeup signal, and receives the oscillation signal from said oscillation circuit and generates a main clock based on the oscillation signal.

20. (Currently Amended) The microcomputer system according to claim 19 ~~21~~, wherein said clock control circuit receives the oscillation signal and outputs the oscillation stop signal based on a condition of the oscillation signal.

21. (Previously Presented) A microcomputer system comprising:

a wakeup signal supplying unit that generates a wakeup signal of a predetermined cycle; and an oscillation circuit which oscillates and outputs an oscillation signal;

a wakeup terminal that receives from outside a wakeup signal of a predetermined cycle; and

a clock control circuit which receives the wakeup signal and the oscillation signal,

wherein said clock control circuit monitors a condition of the oscillation signal and outputs the oscillation stop signal to said oscillation circuit based on the condition of the oscillation signal thereby stopping the oscillations of said oscillation circuit, and wherein said clock control circuit generates a main clock based on the oscillation signal, and,

when said oscillation circuit is not oscillating and when specific time has lapsed, said clock control circuit stops output of the oscillation stop signal to said oscillation circuit based on the wakeup signal.

22. (Currently Amended) The microcomputer system according to claim 21, wherein said clock control circuit outputs the oscillation stop signal when it does not receive the oscillation signal.

23. (New) The microcomputer system according to claim 19, wherein said clock control circuit nullifies the wakeup signal received when the oscillation signal is output from said oscillation circuit.